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METHOD AND/OR APPARATUS FOR DECODING AN INTRA-ONLY MPEG-2 STREAM COMPOSED OF TWO SEPARATE FIELDS ENCODED AS A SPECIAL FRAME PICTURE

Field of the Invention

The present invention relates to video compression generally and, more particularly, to a method and/or apparatus for decoding an intra-only MPEG-2 stream composed of two separate fields encoded as a special frame picture.

Background of the Invention

Referring to FIG. 1, a portion of a typical video frame 10 is shown. The frame 10 includes alternating lines from two separate fields. The separate fields are generally referred to as even/odd, top/bottom, or field1/field2. The vertical resolution of each field is half that of the total video frame. When displayed on a NTSC standard television monitor, each field is shown for one-sixtieth of a second. Due to a characteristic of the human visual system known as persistence, the displayed fields appear to be consecutive and complete frames of motion video.

The frame 10 can be encoded using digital video compression for many applications. Transmission over limited

bandwidth channels such as direct broadcast satellite (DBS) and storage on optical media (i.e., CD, DVD, etc.) are typical examples. In order to achieve efficient compression, complex, computationally intensive processes are used for encoding (or compressing) and decoding (or decompressing) digital video signals. Using conventional digital video compression, the frame 10 can be encoded via a standard such as MPEG-2.

The MPEG-2 compression standard operates on the basis of a variety of rules which eventually act to achieve a representation of the video sequence in a very optimized manner. The application of these specific rules and syntax to a video sequence creates a final stream of bits (i.e., a bitstream) that can be used to accurately replicate the pixels of the original frames of the source image.

MPEG-2 operates on a 16 x 16 pixel block basis. The 16 x 16 block is usually referred to as a macroblock. Macroblocks can have rows (or slices) representing interleaved field lines (e.g., the macroblocks 12 and 14). An MPEG-2 stream containing macroblocks with interleaved field lines is called a frame picture. Alternatively, the macroblocks can have rows representing information from a single field (e.g., the macroblocks 16 and 18).

An MPEG-2 stream containing macroblocks with rows representing information from a single field is called a field picture. The MPEG-2 stream containing macroblocks with rows representing information from a single field occurs in the MPEG-2 syntax traditionally referred to as field picture mode. In the field picture mode, each field of the video frame 10 is encoded separately and converted into a bitstream. Support for field picture mode is mandatory according to the MPEG-2 decoder syntax.

During the encoding process, the video frame 10 can be coded in a fashion that complies with the syntax of the MPEG-2 video frame format, but actually transforms the source video frame to a different representation. One such transformation is when a video frame is comprised of alternating macroblock rows, with each row consisting of 16 vertical lines from each video field. Such a configuration may be advantageous for encoding and transmission of a particular set of video sequences. Additionally, the bitstream can be formed solely of intra-frame pictures. Although such a video frame format can be compressed, it is often desirable that the video sequence be decodable to the normal alternating even/odd field lines for presentation on a television monitor.

A solution for transforming an intra-only, frame picture encoded bitstream into a secondary format that can be decoded as interlaced field pictures by a standard, MPEG-2 compliant decoder would be desirable.

Summary of the Invention

The present invention concerns a method for decoding a bitstream comprising the steps of (A) generating a first field picture in response to a frame picture of a first bitstream, (B) generating a second field picture in response to the frame picture of the first bitstream and (C) generating a second bitstream containing the first field picture and the second field picture.

The objects, features and advantages of the present invention include providing a method and/or apparatus for decoding an intra-only MPEG-2 stream composed of two separate fields encoded as a special frame picture that may (i) transform an intra-only, frame picture encoded bitstream into a secondary format and/or (ii) provide a bitstream format that can be decoded as interlaced field pictures by a standard, MPEG-2 compliant decoder.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a diagram illustrating various encoding schemes for an interlaced video frame;

FIG. 2 is a block diagram illustrating a preferred embodiment of the present invention implemented in a receive path;

FIG. 3 is a block diagram illustrating a transformation block in accordance with a preferred embodiment of the present invention;

FIG. 4 is a more detailed block diagram of a transformation block in accordance with a preferred embodiment of the present invention;

FIG. 5 is a flow diagram illustrating a data flow path in accordance with a preferred embodiment of the present invention; and

FIG. 6 is a flow diagram illustrating a transformation process in accordance with a preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 2, a block diagram of a circuit 100 in accordance with a preferred embodiment of the present invention is shown. The circuit 100 may be implemented, in one example, as a pre-decoder circuit (or block). The circuit 100 may be implemented, in one example, in the context of a receive path 102 of a video transmission system. The circuit 100 may be configured to transform a first bitstream (e.g., BITSTREAM_A) into a second bitstream (e.g., BITSTREAM_B). The bitstream BITSTREAM_A is generally implemented as an MPEG-2 intra-only frame picture bitstream. The bitstream BITSTREAM_A generally comprises alternating macroblock-rows (or slices) containing video information from a single field. The output bitstream BITSTREAM_B generally comprises an intra-only MPEG-2 field picture bitstream.

The receive path 102 may comprise a transmission medium 104 through which a video bitstream may be transmitted. A receiver 106 may receive the bitstream from a transmission medium 104. The receiver 106 may transfer the bitstream to a decode transport system 108. The decode transport system 108 may present the signal BITSTREAM_A to an input of the circuit 100. An output of the circuit 100 may present the signal BITSTREAM_B to an input of a

decoder 110. The decoder 110 may present a decoded video signal to an end user 112. In one example, the decoder 110 may be implemented as a standard MPEG-2 compliant decoder and the end user 112 may be implemented as a standard television monitor. In general, the transmission medium 104, the receiver 106, the decoder transport system 108, the decoder 110 and the end user 112 may be implemented using conventional techniques which are known to those of ordinary skill in the art.

Referring to FIG. 3, a more detailed block diagram of the circuit 100 is shown. In one example, the circuit 100 may comprise a block (or circuit) 120, a buffer 122, a buffer 124 and a block (or circuit) 126. The circuit 120 may be implemented as a transformation block. The circuit 122 and 124 may be implemented as field buffers. In one example, the buffers 122 and 124 may be implemented as separate devices. Alternatively, the buffers 122 and 124 may be implemented as separate portions (or sections of a single memory device. The circuit 126 may be implemented as an output circuit.

The circuit 120 may have an input 128 that may receive the signal BITSTREAM_A. In one example, the signal BITSTREAM_A may be presented to the circuit 120 via a buffer 130. The circuit 120

may be configured to transform the signal BITSTREAM_A from an intra-only MPEG-2 frame picture to individual field data (e.g., a first and a second field picture). The circuit 120 may be further configured to copy sequence related information (e.g, SEQUENCE_RELATED_INFO) from a header of the signal BITSTREAM_A directly to the output signal BITSTREAM_B. The circuit 120 may have an output 132 that may present a signal (e.g., FIELD1) to an input 134 of the buffer 122, an output 133 that may present sequence related information to an input 135 of the output circuit 126 and an output 136 that may present a signal (e.g., FIELD2) to an input 138 of the buffer 124. The signal FIELD1 may comprise a first field header and a number of slices (or rows) containing data of a single field of a video frame. The signal FIELD2 may comprise a second field header and a number of slices comprising data of a second field of a video frame. An output 140 of the buffer 122 and an output 142 of the buffer 124 may be presented to inputs 144 and 146, respectively, of the output circuit 126. The output circuit 126 may be configured to present the sequence related information from the signal BITSTREAM_A, the contents of the buffer 122 and the contents of the buffer 124 consecutively at an output 148 as the signal BITSTREAM_B.

Referring to FIG. 4, a more detailed block diagram of the circuit 120 is shown illustrating an example implementation. The circuit 120 may comprise, in one example, a circuit 150, a circuit 152 and a circuit 154. The circuit 150 may be implemented, in one example, as a header detection and modification circuit. The circuit 152 may be implemented, in one example, as a slice/row demultiplexer circuit (or block). The circuit 154 may be implemented, in one example, as a control circuit.

The signal BITSTREAM_A may be presented to an input of the circuit 150 and an input of the circuit 152. The circuit 150 may be configured to detect a frame header portion of the signal BITSTREAM_A. The header detection and modification circuit 150 may be configured to copy all sequence-related information from the signal BITSTREAM_A to the output 133. The sequence-related information is generally copied without modification. However, in an alternate embodiment, the circuit 150 may be configured to modify one or more portions of any sequence-related headers in the signal BITSTREAM_A prior to presentation at the output 133.

The circuit 150 may be configured to generate a first field header (e.g., an even field header) and a second field header (e.g., an odd field header) in response to the frame header of the

signal BITSTREAM_A. The header detection and modification circuit 150 may be configured to present the first field header as part of the signal FIELD1 and the second field header as part of the signal FIELD2. The circuit 152 may be configured to demultiplex respective slices for the first field (e.g., field 1) and the second field (e.g., field 2) of the frame contained within signal BITSTREAM_A. For example, the circuit 152 may be configured to direct slices for the first field to the signal FIELD1 and slices for the second field to the signal FIELD2. The circuit 154 may be configured to control the circuits 150 and 152. For example, the circuit 154 may be configured to generate one or more control signals for coordinating operation of the circuits 150 and 152 with the signals BITSTREAM_A, FIELD1 and FIELD2.

Referring to FIG. 5, a flow diagram illustrating an example data flow path in accordance with a preferred embodiment of the present invention is shown. In one example, the signal BITSTREAM_A may comprise a frame header 202, a plurality of slices from a first field 204a-204n and a plurality of slices from a second field 206a-206n. The slices 204a-204n and 206a-206n generally alternate position (e.g., are time division multiplexed) in the signal BITSTREAM_A. The frame header 202 is generally

modified to generate a first field header 208 and a second field header 210. A process 212 may be used to modify the frame header 202. In one example, the process 212 may involve copying information of the frame header 202 into each of the field headers 208 and 210 and modifying appropriate fields of the frame header 202 to signal the headers 208 and 210 as being field headers. The slices 204a-204n of field 1 are generally directed to a first field buffer 214. The slices 206a-206n of field 2 are generally directed to a second field buffer 216. The order of the field slices are maintained in the respective field buffers. For example, a picture coding extension field (or portion) of each of the field headers 208 and 210 may be modified from the frame header 202. The slices in each field buffer are generally modified to signal consecutive slice numbers. The field buffers 214 and 216 are generally presented consecutively as the signal BITSTREAM_B.

Referring to FIG. 6, a flow diagram of a process 300 is shown illustrating a transformation process in accordance with a preferred embodiment of the present invention. A bitstream header portion of the signal BITSTREAM_A (e.g., from the start of the bitstream up to the first slice) is generally copied from the signal BITSTREAM_A into a first and a second field buffers (e.g.,

the block 302). A portion (or field) of the bitstream header (e.g., a *picture_coding_extension* field) is generally modified in each of the first and second field buffers to signal a top field picture and a bottom field picture, respectively. Other header parameters may be modified also in accordance with the transformation (e.g., the block 304). The slice rows from the signal BITSTREAM_A are generally de-multiplexed (e.g., alternating copied) to the appropriate field buffer (e.g., the block 306). A field indicative of the slice number for each slice in each field buffer is generally adjusted to increment consecutively in the respective field (e.g., the block 308). When the transformation is complete, the two field buffers are generally written out consecutively to the second signal BITSTREAM_B (e.g., the block 310).

The present invention may be implemented in software, hardware and/or a combination of hardware and software. The function performed by the flow diagrams of FIGS. 5 and 6 may be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled

programmers based on the teachings of the present disclosure, as will also be apparent to those skilled in the relevant art(s).

The present invention may also be implemented by the preparation of application specific integrated circuits (ASICs), application specific standard products (ASSPs), field programmable gate arrays (FPGAs), or by interconnecting an appropriate network of conventional component circuits, as is described herein, modifications of which will be readily apparent to those skilled in the art(s).

The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a computer to perform a process in accordance with the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disk, optical disk, CD-ROM, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, Flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes

in form and details may be made without departing from the spirit and scope of the invention.